

CLAIMS

What is claimed is:

1 1. An method to transform a conditional state element, into a logically redundant
2 element in a digital circuit design comprising:
3 coupling a first latency delay unit to a data input of the conditional state element;
4 coupling a second latency delay unit to an enable input of the conditional state
5 element;
6 coupling a first input of a multiplexer to an output of the conditional state
7 element;
8 coupling a second input of the multiplexer to the data input of the conditional
9 state element; and
10 coupling a select line of the multiplexer to the enable input of the conditional state
11 element.

1 2. The method of claim 1 wherein coupling a first latency delay unit to a data input
2 of the conditional state element comprises coupling a signal with a delay of one unit into
3 the data input of the conditional state element.

1 3. The method of claim 1 wherein coupling a second latency delay unit to an enable
2 input of the conditional state element comprises coupling a signal with a delay of one unit
3 into the data input of the conditional state element.

1 4. The method of claim 1 further comprising replacing the conditional state element
2 in a finite state machine with the logically redundant element said finite state machine
3 having an F function and a G function, coupled to the logically redundant element.

1 5. The method of claim 1 wherein transforming a conditional state element, into a
2 logically redundant element in a digital circuit design comprises transforming any one of
3 a flip-flop, a register file, and a deterministic memory into a logically redundant element.

1 6. The method of claim 4 wherein replacing the conditional state element in a finite
2 state machine with the logically redundant element comprises:

3 coupling the first latency delay unit to an output of the F function;
4 coupling the second latency delay unit to an output of the G function; and
5 coupling the multiplexer output to an input of the F function, and to an input of
6 the G function.

1 7. The method of claim 6 further comprising:

2 adding a first -1 latency delay unit to a latency delay unit coupled to the output
3 of the finite state machine, said latency delay unit not in a feedback loop of the finite state
4 machine;

5 adding a $+1$ latency delay unit and a second -1 latency delay unit between the
6 output of the finite state machine and the data input of the conditional state element;

7 eliminating latency delay units by any one of reduction of the latency delay units
8 and rerouting of the first input of the multiplexer, to automatically create a bypass logic
9 circuit to the finite state machine.

1 8. An apparatus to transform a conditional state element, into a logically redundant
2 element in a digital circuit design comprising:
3 a memory;
4 a processor; and
5 a bus coupled to the memory and the processor, the processor to
6 identify a conditional state element;
7 couple a first latency delay unit to a data input of the conditional state element;
8 couple a second latency delay unit to an enable input of the conditional state
9 element;
10 couple a first input of a multiplexer to an output of the conditional state element;
11 couple a second input of the multiplexer to the data input of the conditional state
12 element; and
13 couple a select line of the multiplexer to the enable input of the conditional state
14 element.

1 9. The apparatus of claim 8 wherein the conditional state element further comprises
2 at least one of a flip-flop, a register file, and a deterministic memory.

1 10. The apparatus of claim 8 wherein the processor to couple a first latency delay unit
2 to a data input of the conditional state element comprises the processor to couple a signal
3 with a delay of one unit into the data input of the conditional state element.

1 11. The apparatus of claim 8 wherein the processor to couple a second latency delay
2 unit to an enable input of the conditional state element comprises the processor to couple
3 a signal with a delay of one unit into the data input of the conditional state element.

1 12. The apparatus of claim 8 further comprising the processor to replace the
2 conditional state element in a finite state machine said finite state machine having an F
3 function and a G function coupled to the logically redundant element.

1 13. The apparatus of claim 12 wherein the processor to replace the conditional state
2 element in a finite state machine with the logically redundant element comprises the
3 processor to:
4 couple the first latency delay unit to an output of the F function;
5 couple the second latency delay unit to an output of the G function; and
6 couple the multiplexer output to an input of the F function, and to an input of the
7 G function.

1 14. The apparatus of claim 13 further comprising the processor to

2 add a first -1 latency delay unit to a latency delay unit coupled to the output of the
3 finite state machine, said latency delay unit not in a feedback loop of the finite state
4 machine;

5 add a $+1$ latency delay unit and a second -1 latency delay unit between the output
6 of the finite state machine and the data input of the conditional state element;

7 eliminate latency delay units by any one of reduction of the latency delay units
8 and rerouting of the first input of the multiplexer, to automatically create a bypass logic
9 circuit to the finite state machine.

1 15. An article of manufacture to transform a conditional state element, into a logically
2 redundant element in a digital circuit design comprising:

3 a machine-accessible medium including instructions that, when executed by a
4 machine, causes the machine to perform operations comprising

5 identifying a conditional state element;

6 coupling a first latency delay unit to a data input of the conditional state element;

7 coupling a second latency delay unit to an enable input of the conditional state
8 element;

9 coupling a first input of a multiplexer to an output of the conditional state
10 element;

11 coupling a second input of the multiplexer to the data input of the conditional
12 state element; and

13 coupling a select line of the multiplexer to the enable input of the conditional state
14 element.

1 16. The article of manufacture of claim 15 wherein said instructions for coupling a
2 first latency delay unit to a data input of the conditional state element comprises further
3 instructions for coupling a signal with a delay of one unit into the data input of the
4 conditional state element.

1 17. The article of manufacture of claim 15 wherein said instructions for coupling a
2 second latency delay unit to an enable input of the conditional state element comprises
3 further instructions for coupling a signal with a delay of one unit into the data input of the
4 conditional state element.

1 18. The article of manufacture of claim 15 further comprising instructions for
2 replacing the conditional state element in a finite state machine with the logically
3 redundant element said *finite state machine* having an F function and a G function,
4 coupled to the logically redundant element.

1 19. The article of manufacture of claim 18 wherein said instructions for replacing the
2 conditional state element in a finite state machine with the logically redundant element
3 comprises further instructions for:
4 coupling the first latency delay unit to an output of the F function;
5 coupling the second latency delay unit to an output of the G function; and
6 coupling the multiplexer output to an input of the F function, and to an input of the G
7 function.

1 20. The article of manufacture of claim 19 comprising further instructions for
2 adding a first -1 latency delay unit to a latency delay unit coupled to the output of
3 the finite state machine, said latency delay unit not in a feedback loop of the finite state
4 machine;
5 adding a $+1$ latency delay unit and a second -1 latency delay unit between the
6 output of the finite state machine and the data input of the conditional state element;
7 eliminating latency delay units by any one of reduction of the latency delay units and
8 rerouting of the first input of the multiplexer, to automatically create a bypass logic
9 circuit to the finite state machine.